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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,880	03/30/2004	Koji Hirosawa	57810-097	2498

7590 12/10/2008

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EXAMINER	
SITTA, GRANT	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
12/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,880	HIROSAWA, KOJI	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-7, 10-18, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon et al (7,106,292) hereinafter, Moon in view of Jeon et al (6,690,347) hereinafter, Jeon.

4. In regards to claim 1, Moon discloses the limitations of a plurality of stages of shift register circuits (fig. 16, SRC1-SRC4) for sequentially driving (col. 5, lines 50-60) a plurality of drain lines for supplying a video signal to pixels (fig. 16 Vdis); and

first dummy shift register circuit arranged on the operation starting side of said plurality of stages of shift register circuits and not connected to said drain line (fig. 16 dummy stage 0). Examiner notes that Moon does disclose using a plurality of dummy

shift registers circuits on the operation starting side but does disclose using a plurality of dummy shift registers one at the operation start side and one dummy shift register at the end (fig. 16 (dummy stage 0 and dummy stage 1)).

Moon differs in that Moon does not teach a plurality of stages of first dummy shift register circuits arranged at the operation starting side.

However, to duplicate parts for multiplied effect is generally considered obvious to one of ordinary skill in the art. *St. Regis Paper Co. v. Bemis Co.*, Inc. 193 USPQ 8, 11 (7th Cir. 1977).

It would have been obvious to one of ordinary skill in the art to provide a plurality of dummy shift registers a plurality of stages of first dummy shift register circuits arranged at the operation starting side because if one dummy shift register circuit reduces penetration current that causes display irregularities than two dummy shift register circuits would further reduce display irregularities.

Moon also differs from the claimed invention in that Moon does not disclose wherein said shift register circuits and said first dummy shift register circuits include a first circuit section having a first transistor of first conductivity type whose drain/source is connected to a first fixed potential, a second transistor of first conductivity type whose drain/source is connected to the source/drain of said first transistor and whose source/drain is connected to a second fixed potential, and a third transistor of first conductivity type whose drain/source is connected to a gate of said first transistor and whose source/drain is connected to said second fixed potential for turning off said first transistor when said second transistor is in on state.

However, Jeon teaches a system and method for wherein said shift register circuits and said first dummy shift register circuits include a first circuit section having a first transistor of first conductivity type whose drain/source is connected to a first fixed potential (fig. 7 (NT1) col. 11, line 39)), a second transistor of first conductivity type whose drain/source is connected to the source/drain of said first transistor and whose source/drain is connected to a second fixed potential (fig. 7 NT2 col. 11 line 45), and a third transistor of first conductivity type whose drain/source is (fig. 7 NT4 col. 11, lines 53-55) connected to a gate of said first transistor and whose source/drain is connected to said second fixed potential for turning off said first transistor when said second transistor is in on state (col. 13, lines 5-21 of Jeon).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Moon to include the use of the shift register configuration as taught by Jeon in order to sequentially and stably generate outputs as stated in (col. 13, lines 34-37 of Jeon).

5. In regards to claim 11, Moon discloses the limitations of a plurality of stages of shift register circuits for sequentially driving a plurality of drain lines for supplying a video signal to pixels (col. 2, lines 48-67); and

a plurality of stages of dummy shift register circuits arranged by said plurality of stages of shift register circuits and not connected to said drain line (fig. 16 dummy stage 0 and dummy stage 1).

Moon differs in that Moon does not teach a plurality of stages of first dummy shift register circuits arranged at the operation starting side and not connected to said drain line.

However, to duplicate parts for multiplied effect is generally considered obvious to one of ordinary skill in the art. *St. Regis Paper Co. v. Bemis Co.*, Inc. 193 USPQ 8, 11 (7th Cir. 1977).

It would have been obvious to one of ordinary skill in the art to provide a plurality of dummy shift registers a plurality of stages of first dummy shift register circuits arranged at the operation starting side because if one dummy shift register circuit reduces penetration current that causes display irregularities than two dummy shift register circuits would further reduce display irregularities.

Moon also differs from the claimed invention in that Moon does not disclose wherein said shift register circuits and said first dummy shift register circuits include a first circuit section having a first transistor of first conductivity type connected to a first fixed potential, a second transistor of first conductivity type connected to a second fixed potential, and a third transistor of first conductivity type connected between a gate of said first transistor and whose source/drain is connected to said second fixed potential for turning off said first transistor when said second transistor is in on state; and

wherein said first circuit section includes a fourth transistor of first conductivity type connected to the gate of said first transistor and operated to turn on in response to a first signal, and a fifth transistor of first conductivity type connected between said

fourth transistor and said first fixed potential and operated to turn on in response to a second signal turned off when said first signal is in on state.

However, Jeon teaches a system and method for wherein said shift register circuits and said first dummy shift register circuits include a first circuit section having a first transistor (fig. 7 NT1) of first conductivity type connected to a first fixed potential (fig. 7 CK), a second transistor (fig. 7 NT2) of first conductivity type connected to a second fixed potential (fig. 7 VSS), and a third transistor (fig. 7 NT4) of first conductivity type connected between a gate of said first transistor and whose source/drain (col. 11, lines 50-55) is connected to said second fixed potential for turning off said first transistor when said second transistor is in on state(col. 13, lines 5-21 of Jeon); and

wherein said first circuit section includes a fourth transistor (fig. 7 NT3) of first conductivity type connected to the gate of said first transistor and operated to turn on in response to a first signal (fig. 7 IN), and a fifth transistor (fig. 7 NT5) of first conductivity type connected (fig. 7 N1) between said fourth transistor (fig. 7 NT3) and said first fixed potential (fig. 7 CK) and operated to turn on in response to a second signal turned off when said first signal is in on state. (fig. 6 and fig. 8 CT and Out1) since the outputs are sequential NT3 is operated to turn on in response to a CT signal turned off when said first signal ,ST, is in on state. Examiner notes that ST is the start signal for the first stage that is applied the shift registers).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Moon to include the use of the shift register configuration as taught

by Jeon in order to sequentially and stably generate outputs as stated in (col. 13, lines 34-37 of Jeon).

6. In regards to claim 13, Moon discloses the limitations of a plurality of stages of shift register circuits (fig. 16, SRC1-SRC4) for sequentially driving (col. 5, lines 50-60) a plurality of drain lines for supplying a video signal to pixels (fig. 16 Vdis); and

a dummy shift register circuit arranged on the operation starting side of said plurality of stages of shift register circuits and not connected to said drain line (fig. 16 dummy stage 0).

Moon differs from the claimed invention in that Moon does not disclose wherein said shift register circuits and said dummy shift register circuits include a first circuit section having a first transistor of first conductivity type whose drain/source is connected to a first fixed potential, a second transistor of first conductivity type whose drain/source is connected to the source/drain of said first transistor and whose source/drain is connected to a second fixed potential, and a third transistor of first conductivity type whose drain/source is connected to a gate of said first transistor and whose source/drain is connected to said second fixed potential for turning off said first transistor when said second transistor is in on state.

However, Jeon teaches a system and method for wherein said shift register circuits and said dummy shift register circuits include a first circuit section having a first transistor of first conductivity type whose drain/source is connected to a first fixed potential (fig. 7 (NT1) col. 11, line 39)), a second transistor of first conductivity type

whose drain/source is connected to the source/drain of said first transistor and whose source/drain is connected to a second fixed potential (fig. 7 NT2 col. 11 line 45), and a third transistor of first conductivity type whose drain/source is (fig. 7 NT4 col. 11, lines 53-55) connected to a gate of said first transistor and whose source/drain is connected to said second fixed potential for turning off said first transistor when said second transistor is in on state (col. 13, lines 5-21 of Jeon).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Moon to include the use of the shift register configuration as taught by Jeon in order to sequentially and stably generate outputs as stated in (col. 13, lines 34-37 of Jeon).

7. In regards to claim 22, Moon discloses the limitations of a plurality of stages of shift register circuit (fig. 16, SRC1-SRC4) for sequentially driving (col. 5, lines 50-60) a plurality of drain lines for supplying a video signal to pixels (fig. 16 Vdis); and

a dummy shift register circuits arranged on the operation starting side of said plurality of stages of shift register circuits and not connected to said drain line (fig. 16 dummy stage 0).

Moon differs from the claimed invention in that Moon does not disclose wherein said shift register circuits and said dummy shift register circuits include a first circuit section having a first transistor of first conductivity type whose drain/source is connected to a first fixed potential, a second transistor of first conductivity type whose drain/source is connected to the source/drain of said first transistor and whose

source/drain is connected to a second fixed potential, and a third transistor of first conductivity type whose drain/source is connected to a gate of said first transistor and whose source/drain is connected to said second fixed potential for turning off said first transistor when said second transistor is in on state.

wherein said first circuit section includes a fourth transistor of first conductivity type connected to the gate of said first transistor and operated to turn on in response to a first signal, and a fifth transistor of first conductivity type connected between said fourth transistor and said first fixed potential and operated to turn on in response to a second signal turned off when said first signal is in on state.

However, Jeon teaches a system and method for wherein said shift register circuits and said dummy shift register circuits include a first circuit section having a first transistor of first conductivity type whose drain/source is connected to a first fixed potential (fig. 7 (NT1) col. 11, line 39)), a second transistor of first conductivity type whose drain/source is connected to the source/drain of said first transistor and whose source/drain is connected to a second fixed potential (fig. 7 NT2 col. 11 line 45), and a third transistor of first conductivity type whose drain/source is (fig. 7 NT4 col. 11, lines 53-55) connected to a gate of said first transistor and whose source/drain is connected to said second fixed potential for turning off said first transistor when said second transistor is in on state (col. 13, lines 5-21 of Jeon).

wherein said first circuit section includes a fourth transistor (fig. 7 NT3) of first conductivity type connected to the gate of said first transistor and operated to turn on in response to a first signal (fig. 7 IN), and a fifth transistor (fig. 7 NT5) of first conductivity

type connected (fig. 7 N1) between said fourth transistor (fig. 7 NT3) and said first fixed potential (fig. 7 CK) and operated to turn on in response to a second signal turned off when said first signal is in on state. (fig. 6 and fig. 8 CT and Out1) since the outputs are sequential NT3 is operated to turn on in response to a CT signal turned off when said first signal, ST, is in on state. Examiner notes that ST is the start signal for the first stage that is applied the shift registers).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Moon to include the use of the shift register configuration as taught by Jeon in order to sequentially and stably generate outputs as stated in (col. 13, lines 34-37 of Jeon).

8. In regards to claim 2, Moon as modified by Jeon teaches further comprising a second dummy shift register circuit arranged on the side opposite to the operation starting side of said plurality of stages of shift register circuits and not connected to said drain line (fig. 16 DUMMY STAGE 1 Moon).

9. In regards to claim 3, Moon as modified by Jeon teaches wherein a start signal is input to the first stage of said plurality of stages of first dummy shift register circuits (fig. 16 STV Moon).

10. In regards to claim 4, Moon as modified by Jeon teaches NMOS transistors (col. 3, line 30 of Jeon).

Moon and Jeon differ from the claimed invention in that Moon and Jeon does not expressly disclose wherein at least said first transistor, said second transistor and said third transistor are a p- type field effect transistor.

At the time of the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to replace NMOS transistors with PMOS transistors since they are often considered interchangeable with minor modifications made to the circuit. Applicant has not disclosed that p- type field effect transistor or PMOS provides an advantage, is used for a particular purpose, or solves a stated problem. On of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with NMOS transistors because all that is changed is the direction of current flowing in the inversion layer of the transistor.

Therefore, it would have been an obvious matter of design choice to modify Moon and Jeon to obtain the invention as specified claim 4.

11. In regards to claim 5, Moon as modified by Jeon teaches wherein a first capacitor is connected between the gate and a source of said first transistor (fig. 7 (C) Jeon).

12. In regards to claim 6, Moon as modified by Jeon teaches wherein said third transistor has two gate electrodes electrically connected to each other (fig. 7 NT4 and NT2) Jeon).

13. In regards to claim 7, Moon as modified by Jeon teaches wherein said first transistor is turned on in response to a clock signal (fig. 8 ST is a clock Jeon).

14. In regards to claim 10, Moon as modified by Jeon teaches wherein said first circuit section further includes a fifth transistor (fig. 7 NT5 Jeon) of first conductivity type connected (fig. 7 N1 Jeon) between said fourth transistor (fig. 7 NT3 Jeon) and said first fixed potential (fig. 7 CK) and operated to turn on in response to a second signal turned off when said first signal is in on state. (fig. 6 and fig. 8 CT and Out1 Jeon) since the outputs are sequential NT3 is operated to turn on in response to a CT signal turned off when said first signal, ST, is in on state. Examiner notes that ST is the start signal for the first stage that is applied the shift registers).

15. In regards to claim 12, Moon as modified by Jeon teaches wherein a capacitor is connected between a source of said first transistor and a junction point between said fourth transistor and said fifth transistor (fig. 7 (C) Jeon).

16. In regards to claim 14, Moon as modified by Jeon differ in that Moon and Jeon do not teaches two stages of dummy shift register circuits not connected to said drain line and arranged on the operation starting side of said plurality of stages of shift register circuits.

However, to duplicate parts for multiplied effect is generally considered obvious to one of ordinary skill in the art. *St. Regis Paper Co. v. Bemis Co.*, Inc. 193 USPQ 8, 11 (7th Cir. 1977).

I t would have been obvious to one of ordinary skill in the art to provide a plurality of dummy shift registers a plurality of stages of first dummy shift register circuits arranged at the operation starting side because if one dummy shift register circuit reduces penetration current that causes display irregularities than two dummy shift register circuits would further reduce display irregularities.

17. In regards to claim 15, Moon as modified by Jeon teaches NMOS transistors (col. 3, line 30 of Jeon).

Moon and Jeon differ from the claimed invention in that Moon and Jeon does not expressly disclose wherein at least said first transistor, said second transistor and said third transistor are a p- type field effect transistor.

At the time of the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to replace NMOS transistors with PMOS transistors since they are often considered interchangeable with minor modifications made to the circuit. Applicant has not disclosed that p- type field effect transistor or PMOS provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with NMOS transistors because all that is changed is the direction of current flowing in the inversion layer of the transistor.

Therefore, it would have been an obvious matter of design choice to modify Moon and Jeon to obtain the invention as specified claim 15.

18. In regards to claim 16, Moon as modified by Jeon teaches wherein a first capacitor is connected between the gate and a source of said first transistor (fig. 7 (C) Jeon).

19. In regards to claim 17, Moon as modified by Jeon teaches wherein said third transistor has two gate electrodes electrically connected to each other (fig. 7 NT4 and NT2) Jeon).

20. In regards to claim 18, Moon as modified by Jeon teaches wherein said first transistor is turned on in response to a clock signal (fig. 7 ST is a clock signal Jeon).

21. In regards to claim 21, Moon as modified by Jeon teaches wherein said first circuit section further includes a fifth transistor (fig. 7 NT5 Jeon) of first conductivity type connected (fig. 7 N1 Jeon) between said fourth transistor (fig. 7 NT3 Jeon) and said first fixed potential (fig. 7 CK) and operated to turn on in response to a second signal turned off when said first signal is in on state. (fig. 6 and fig. 8 CT and Out1 Jeon) since the outputs are sequential NT3 is operated to turn on in response to a CT signal turned off when said first signal, ST, is in on state. Examiner notes that ST is the start signal for the first stage that is applied the shift registers).

22. In regards to claim 23, Moon as modified by Jeon teaches wherein a capacitor is connected between a source of said first transistor and a junction point between said fourth transistor and said fifth transistor (fig. 7 (C) Jeon).

23. Claims 8, 9, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon in view of Jeon, and further in view of Hebiguchi et. al (US 6,295,046) hereinafter Hebiguchi.

24. In regards to claims 8 and 19 Moon and Jeon differ from the claimed invention in that Moon and Jeon do not disclose a diode-connected transistor between the gate of the first transistor and a clock signal.

However, Hebiguchi teaches a system and method for including a diode-connected transistor between the gate of the first transistor and a clock signal (Fig. 7 col. 5, lines 45-55 of Hebiguchi).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Moon to include the use of a diode-connected transistor as taught by Hebiguchi in order to resist noise interference as stated in (Fig. 7 col. 5, lines 45-55 of Hebiguchi).

25. In regards to claims 9 and 20, Moon in view of Jeon as modified by Hebiguchi discloses wherein said diode-connected fourth transistor has two gate electrodes

electrically connected to each other (Fig. 7 "2" and the gate of the diode-connected transistor of Hebiguchi).

Response to Arguments

26. Applicant's arguments filed 09/09/2008 have been fully considered but they are not persuasive.

27. In response to Applicant's remarks that the prior art of record fails to teach wherein the first transistor is connected to a fixed potential. (Remarks, page 10, last paragraph). Examiner respectfully disagrees. First, examiner contends that the potential is fixed because it is a clock. Microsoft Computer Dictionary Fifth edition, Microsoft Press, Published 05/01/2002. Defines clock n. 1. The electronic circuit in a computer that generates a steady stream of timing pulses--the digital signals that synchronize every operation. The steady stream is a fixed potential (i.e. the potential is fixed in that the signal is 5 volts for 3 ms, then 0 volts for 3ms, 5 volts for 3 ms, etc.).

28. Second, for sake of argument, a clock signal is formed by switching between two constant potentials. Thus, the first transistor would still be connected to a fixed potential either way the claim language is viewed.

29. For the reason set forth above, the current claim language has not distinguished itself from the prior art of record.

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

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Examiner, Art Unit 2629
December 4, 2008